Pune Vidyarthi Griha's

COLLEGE OF ENGINEERING, NASHIK – 4

COMPUTER ENGINEERING DEPARTMENT

Subject : DELD **ASSIGNMENT NO – 03** **Unit : III**

1. What is ASM? State & explain basic component of ASM Chart. Features of ASM.
2. Draw an ASM Chart & state table of a 2-bit up-down counter having a mode control i/p.
3. Draw the ASM Chart & state diagram for Synchronous circuit having the following description : The circuit has control input C, Clock & Output x, y, z.
   i. If C = 1 Then changes from 000→010→100→110→000 & Repeats
   ii. If C = 0 Then circuit holds the present state.
4. Explain the Mux Controller Method with an example?
5. A sequential circuit has to count DOWN from '111' to '000'. The circuit also has input 'X'. If X = 0 then the circuit will count DOWN and if X = 1 then they will remain in current state. Draw an ASM Chart and state table for this circuit and design the circuit to generate the output using MUX Controller method.
6. Draw ASM Chart for the following state machine : A two bit UP Counter with output 'Q1Q0' and enable signal 'X' is to be designed. If 'X' = 0 counter changes the state as '00 – 01 – 10 – 11 – 00'. If 'X' = 1 , counter should remain in present state. Design your circuit using JK-FF and suitable MUXs.
7. Design ASM Chart for 4-bit gray code sequence with up-down conditions.
8. Design ASM Chart for 3-bit octal number sequence with up-down condition.
9. Design a sequence generator circuit to generate the sequence 1 – 3 – 5 – 7 using MUX Controller based ASM approach. Consideration :
   i. If C = 0 Then the sequence generator circuit in the same state
   ii. If C = 1 Then the sequence generator circuit goes into next state.

10. Design a sequence generator circuit to generate the sequence 1 – 2 - 3 – 7 - 1 using MUX Controller based ASM approach. Consideration :
    iii. If C = 0 Then the sequence generator circuit in the same state
    iv. If C = 1 Then the sequence generator circuit goes into next state.
11. What is VHDL? Features of VHDL and its advantages.
12. State the VHDL Program format & entity format. Explain the entity declaration for basic logic gate and Universal gates.
13. Explain the entity architecture declaration for 2-bit AND, OR, NOR gate.
14. Describe the different Modeling Styles of VHDL with suitable examples.
15. Comparison between dataflow, behavioral and structural modeling.
16. Compare concurrent Vs sequential statements.
17. Write VHDL code for 4:1 MUX. AND Full Adder.

********** **Best of Luck** **********